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UTILITY PATENT APPLICATION TRANSMITTAL
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(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. 55058(820)

Total Pages in this Submission 35

TO THE ASSISTANT COMMISSIONER FOR PATENTS
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Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD FOR FABRICATING METAL WIRINGS

and invented by:

YOSHIMASA CHIKAMA, YOSHIHIRO IZUMI

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having 32 pages and including the following:

   a. ☒ Descriptive Title of the Invention

   b. ☐ Cross References to Related Applications *(if applicable)*

   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*

   d. ☐ Reference to Microfiche Appendix *(if applicable)*

   e. ☒ Background of the Invention

   f. ☒ Brief Summary of the Invention

   g. ☒ Brief Description of the Drawings *(if drawings filed)*

   h. ☒ Detailed Description

   i. ☒ Claim(s) as Classified Below

   j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 3
   b. ☐ Informal Number of Sheets

4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☒ Certificate of Mailing
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Accompanying Application Parts (Continued)

15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
Certified Copies of Japanese Patent Application Nos. 11-239682, Filed 8/26/99 and 2000-205190, Filed 7/6/00

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

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For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	14	- 20 =	0	x	$18.00	$0.00
Indep. Claims	1	- 3 =	0	x	$78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
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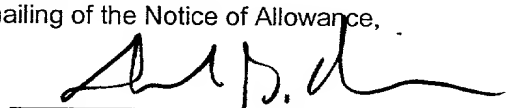

Signature

Dated: **August 25, 2000**

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Invention:

METHOD FOR FABRICATING METAL WIRINGS

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METHOD FOR FABRICATING METAL WIRINGS

BACKGROUND OF THE INVENTION

The present invention relates to a method for fabricating metal wirings used for flat panel displays such as liquid crystal displays (LCDs), plasma display panels (PDPs), electrochromic displays (ECDs) and electroluminescent displays (ELDs), printed wiring boards using ceramic boards, and other various fields.

Conventionally, in a flat panel display typified by LCDs, normally, display material such as liquid crystals is held between a pair of substrates and a voltage is applied to this display material. In this case, electrical wiring lines are arrayed on at least one of the substrates.

For example, in the case of an active matrix drive type LCD, on one of a pair of substrates constituting part of a display unit, gate electrodes and data electrodes are disposed in a matrix shape, and thin film transistors (TFTs) and pixel electrodes are disposed at individual intersections of these electrodes. Normally, these gate electrodes and data electrodes are made of a metal material such as Ta, Al or Mo, and deposited by a dry film formation process such as sputtering process.

In such flat panel displays, in an attempt to implement larger areas and higher definitions, the drive

frequency would increase while the electric wiring resistance as well as the parasitic capacitance would increase. As a result of this, delay of driving signals would come up as a large problem.

Thus, in order to solve the problem of the delay of driving signals, there have been made attempts to use Cu (bulk resistivity: 1.7 μΩ·cm), which is lower in electrical resistance, instead of Al (bulk resistivity: 2.7 μΩ·cm), α-Ta (bulk resistivity: 13.1 μΩ·cm) or Mo (bulk resistivity: 5.8 μΩ·cm), which are conventional wiring materials. For example, "Low Resistance Copper Address Line for TFT-LCD" (Japan Display '89, pp. 498 - 501) discloses discussion results on a case of using Cu as the gate electrode material of TFT-LCDs. According to this literature, it is expressly described out that because a Cu film deposited by sputtering process is poor in adhesion with the ground glass, a metal film of Ta or the like needs to be interveniently provided as a ground film in order to enhance the adhesion.

However, in the case of the wiring structure in which a metal film of Ta or the like is provided as the ground, dry formation processes and etching processes would be involved individually for the Cu film and the ground metal film of Ta or the like, causing a process increase and leading to a cost increase, as a disadvantage.

Thus, in Japanese Patent Laid-Open Publication HEI 4-232922, there has been proposed a method in which while a transparent electrode made of ITO (Indium-Tin-oxide) or the like is used as a ground film, a metal film of Cu or the like is formed by plating technique on the ground film. In this technique, it is expressly described that since the plated metal can be formed selectively only on the ITO film, the patterning process is required only for the ITO film of the transparent electrode so that Cu wiring can effectively be formed even for large areas. The publication also describes that a metal film of Ni or the like having good adhesion with the ITO film is interveniently provided between the ITO film and Cu wiring.

On the other hand, in addition to the electrical wiring fabricating method described in Japanese Patent Laid-Open Publication HEI 4-232922, there have been proposed electrical wiring fabricating methods in which a film of Ni, Au, Cu or other metal is formed on a patterned ITO film by plating technique for various purposes such as the process reduction for the active matrix substrate, lower resistance of the transparent conductive film in simple matrix type LCDs or the like, and improvement solder wettability on the ITO film (see, e.g., Japanese Patent Laid-Open Publications HEI 2-83533, HEI 2-223924, HEI 1-96383, SHO 62-288883).

However, in the case where the Cu/Ta lamination film is formed by sputtering process, i.e., where both the Cu film for lower resistance and the ground metal film intended to improve the adhesion with the Cu film are formed by vacuum deposition equipment, individual film deposition processes are involved for the Cu film and the ground metal film, respectively, causing a process increase and leading to a cost increase, as a disadvantage. Also, individual etching processes are involved for the Cu film and the ground metal film, respectively, causing a process increase and leading to a cost increase, as a disadvantage.

Also, in the electrical wiring fabricating method in which ITO is used for the ground metal film, because the metal film is formed by wet formation technique while the ITO film is formed by vacuum deposition equipment for sputtering process, vapor deposition process or the like, enough cost reduction effect cannot be obtained, resulting in a problem that large-scale substrates cannot be easily managed.

SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide an electrical wiring fabricating method capable of fabricating the electrical wiring with low cost without

using any vacuum deposition and managing large-scale substrates.

In order to achieve the above object, the present invention provides a method for fabricating metal wirings, comprising the steps of:

forming a ground resin film by applying a resin onto an insulating substrate;

patterning the ground resin film; and

forming a low-resistance metal film selectively on the patterned ground resin film by a wet film formation technique.

According to this invention, the ground resin film can be formed by spin coating, like resist or the like. The low-resistance metal film provided thereon can be formed selectively on the ground resin film by a wet film formation technique. Therefore, the need for vacuum deposition equipment, etching equipment or the like is eliminated.

As a result, it becomes possible to form metal wirings without using any vacuum deposition equipment, thus allowing a considerable cost reduction to be achieved as compared with the case where electrical wirings are formed by the method shown in the prior art example.

Also, since the ground film is made of resin, the film having good adhesion can be easily formed on the insulating substrate.

Further, since a wet film formation technique is used for film formation, the film formation can be achieved only by immersing the substrate into a solution, thus easily coping with large-scale substrates.

The wet film formation technique herein referred to is a technique that film formation is done by immersing the substrate into a solution without using any vacuum equipment, the technique being exemplified by plating process, electrolytic process, dip coating process, coating process or the like. In addition, such a film formation technique as shown in later-described Japanese Patent Laid-Open Publication HEI 10-245444 is also included in the scope of the wet film formation technique.

In one embodiment, the ground resin film is made of a photosensitive resin that can be patterned by exposure and development.

According to this embodiment, in addition to the foregoing effects, it becomes possible to easily form a high-definition film, as in the case of photoresist that is currently used. By using such a resin as those used for printed wiring boards, the ground resin film can be provided as a ground film that allows a single low-resistance metal film of, for example, Cu to be formed with good adhesion.

In one embodiment, the low-resistance metal film is a single layer film containing any one of Cu, Ni and Au

or a multilayer film containing at least one of these single layers.

According to this embodiment, the low-resistance metal film is made of Cu, which has characteristics of low resistivity (bulk resistivity: 1.7 μΩ·cm) and long life against electromigration, thus optimum as a wiring material.

Also, even with low adhesion between Cu and ground resin, low-resistance wirings of good adhesion with the ground resin can be achieved by using Ni of good adhesion as the ground and forming Cu/Au or the like thereon.

In one embodiment, the ground resin film is made of polyimide.

Since polyimide is superior in heat resistance and chemical resistance among resins, using polyimide as the ground resin as in the metal wiring fabricating method of this embodiment allows a manufacturing method to be chosen from a wide variety of methods for the processes subsequent to the formation of the ground resin film.

For example, when plating process is used as the wet film formation process for forming the low-resistance metal film, the plating solution is in many cases strong alkali or strong acid. Therefore, high chemical resistance is effective for that process.

Also, polyimide, because of its high heat resistance, allows the margin for other film formation

processes to be widely taken. For example, while the process maximum temperature for normal amorphous liquid crystals is about 350°C, polyimide has a heat resistance of about 400°C (polyimide is normally thermally cured at about 350°C; thermal decomposition temperature of polyimide is, in many cases, not less than 450°C). Therefore, unlike the cases where other resins are used, there is no need of lowering the process temperature. The unnecessity of process change prevents occurrence of failures that would be involved in necessity of process changes, thus giving a large advantage for manufacture of products.

In addition, thermal resistance temperature of other resins is about 200°C for normal resist that is used for liquid crystals, and not more than 250°C for acrylic resin.

Also, some photosensitive polyimides have a resolution of L/S = 5 μm or more, which is a satisfactory resolution as the ground material of the low-resistance metal for forming metal wirings.

Also, plated copper on polyimide has been already put into practical use in the field of printed boards or the like, thus satisfactory as the ground film in view of using plating process as the wet film formation technique.

In one embodiment, plating is used as the wet film formation technique, and the ground resin contains a plating catalyst.

According to this embodiment, since the plating catalyst is contained, it becomes possible to use a resin to which it is hard to selectively impart the plating catalyst.

Also, in the case of a resin that allows the plating catalyst to be easily imparted thereto, the step of imparting the catalyst during the plating process can be omitted, thus allowing process reduction to be easily achieved, as an advantage.

One embodiment further comprises a step for, before the step of forming the low-resistance metal film, modifying a surface of the ground resin film.

According to this embodiment, the surface of the ground resin film is modified, thereby forming asperity on the surface of the ground resin film. By the asperity formed on the surface of the ground resin film, the adhesion between the ground resin film and the low-resistance metal film can be improved to such an extent as could not be obtained by the catalyst imparting method used as a pre-processing for conventional plating process.

Also, as the surface of the modified ground resin film is highly capable of adsorbing metal ions, reducing these metal ions allows a metal layer to be obtained on the

surface of the ground resin film. That is, a metal film that acts as a catalyst in the process of forming the low-resistance metal film can be formed selectively on the ground resin film without adding any patterning process such as photolithography process.

One embodiment further comprises a step for, after the step of modifying the surface of the patterned ground resin film, forming on the surface-modified ground resin film a metal layer serving as a catalyst in the process of forming the low-resistance metal film by the wet film formation technique.

According to this embodiment, a metal layer is formed on the ground resin film. This metal layer acts as a catalyst in the process of forming the low-resistance metal film on the ground resin film by, for example, electroless plating process as a wet film formation process. Since the metal layer is easily formed on the modified ground resin film as described above, resin materials to which the plating catalyst is hard to selectively impart become usable as the ground resin, thus allowing the material of the ground resin film to be chosen from a wider variety of materials, so that the material cost of the ground resin becomes lower. Also, since the step of imparting the catalyst in the plating process can be omitted even with the use of a resin to which a plating catalyst is easily

imparted, the metal wiring manufacturing processes can be reduced.

In one embodiment, the step of forming the metal layer acting as a catalyst in the process of forming the low-resistance metal film by the wet film formation technique comprises the steps of:

making metal ions adsorbed onto the surface-modified ground resin film; and

reducing the metal ions.

According to this embodiment, after metal ions are adsorbed to the ground resin film, the metal layer is formed by reducing the metal ions. That is, without using any dry film deposition technique or etching technique, the metal layer is formed selectively on the ground resin film with ease and lower cost. As a result, the fabrication of the metal wirings is facilitated while the fabrication cost for the metal wirings is reduced.

In one embodiment, the step of modifying the surface of the patterned ground resin film is a process using KOH (Potassium hydroxide).

According to this embodiment, even when the ground resin film is made of a material having strong chemical resistance such as polyimide, an etching process is done with KOH. Therefore, asperity is formed on the surface of the ground resin film, so that a good adhesion of the ground

resin film with the low-resistance metal film can be obtained and that the metal ions can be adsorbed enough.

In one embodiment, the metal ions to be adsorbed onto the surface-modified ground resin film are any one of Cu, Ag and Pd ions.

According to this embodiment, these metal ions serve as a catalyst in the process of forming the low-resistance metal film by electroless plating as an example of the wet film formation technique, there is no need of imparting any catalyst for the plating process, so that the process for forming the low-resistance metal film can be reduced. Also, all these metal ions serve as a plating catalyst for the process of forming a low-resistance metal film of, for example, Cu on the ground resin film, the metal ions can be selected depending on the kind of the ground resin film or the conditions for the plating process.

In one embodiment, the step of reducing the metal ions is a process in which ultraviolet rays are irradiated to places where the low-resistance metal film is to be formed, by which the metal ions are selectively reduced.

According to this embodiment, the metal ions are reduced by irradiating ultraviolet rays, there is no need for a reducing agent, and so the liquid waste processing that would be involved in the use of a reducing agent is no longer necessary. Thus, the material cost for the reducing

agent or the like and the liquid waste processing cost are reduced, so that the fabrication of metal wirings become easier and lower in price.

Further, the metal layer that serves as a catalyst in the process of forming the low-resistance metal film can be selectively formed by selectively reducing the metal ions of the ground resin film with the use of, for example, a mask. In this case, it becomes possible to form low-resistance metal film of different patterns on the patterned ground resin film.

The ground resin film to be formed in the present invention is preferably formed into a thickness of 0.05 - 0.5 μm. For example, in the case where metal wirings for an active matrix drive type LCD or the like are formed according to the present invention, if the ground resin film is thicker, there would occur such problems as disconnections at wiring jumping portions or occurrence of cracks at edge portions. With regard to the metal wirings of this active matrix drive type LCD, the total thickness of the metal wirings is desirably 0.5 - 0.8 μm at most, and therefore the thickness of the ground resin film is desirably not more than 0.5 μm at most. However, if the ground resin film is too thin, there would occur such problems as lowered adhesion between ground resin and insulating substrate, or dissipation of the ground resin

film due to uniformities of etching depth in the etching process. Therefore, the thickness of the ground resin film is desirably not less than 0.05 μm.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

Figs. 1A, 1B, 1C are process diagrams showing a method for fabricating metal wirings according to a first embodiment of the invention;

Fig. 2 is a sectional view of a thin film transistor (TFT) in which the metal wirings obtained by the manufacturing flow shown in Figs. 1A - 1C are applied to an active matrix substrate; and

Figs. 3A, 3B, 3C are process diagrams showing a method for fabricating metal wirings according to a third embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinbelow, a metal wiring fabricating method of the present invention is described in detail by way of

embodiments thereof illustrated in the accompanying drawings.

These embodiments are explained on the assumption that the metal wiring fabricating method of the invention is applied to the manufacture of an active matrix drive type LCD.

(First Embodiment)

Figs. 1A - 1C are process diagrams of a first embodiment of the metal wiring fabricating method of the invention, where electroless plating is used as the wet film formation technique. In this case, a glass substrate (Corning 1373 Glass made by Corning Inc.) was used as an insulating substrate 1. It is noted that the insulating substrate referred to in this specification includes inorganic substrates such as glass substrates, ceramic substrates and semiconductor substrates or conductor substrates equipped with an insulating layer on the top surface, as well as various types of organic substrates or films of PET (Polyethylene Terephthalate), ABS (Alkylbenzene Sulphonate), PC (Polycarbonate) and the like. As the ground resin film, photosensitive polyimide (HD-6000 made by Hitachi Chemical - Du Pont) was used.

(First Step)

At this first step, as shown in Fig. 1A, a ground resin film 2 is formed by coating process on a top of the insulating substrate 1.

First, the top surface of the insulating substrate 1 is degreased and cleaned by alkali or acid or organic solvent. In this cleaning process, using ultrasonic waves in combination is effective. Then, after the insulating substrate 1 is dried, photosensitive polyimide is applied to a thickness of about 1.5 μm by using a spin coating application method, and further pre-baked (at 85°C for 120 seconds), by which a ground resin film 2 is formed. In the active matrix drive type LCD, since the thickness of the whole metal wirings is desirably 0.5 - 0.8 μm at most, the thickness of the resin portion is desirably not more than 0.5 μm at most. The thinner the ground resin film 2 is, the thinner the metal wirings can be made and the better the resulting taper configuration becomes.

However, the resin portion may be made thick in cases where thicker film thicknesses are desired.

In addition, the ground resin referred to in this case may be made of novolak resin that is used as resist, polyimide-base or acrylic resin, epoxy resin that is used as printed wiring boards, and the like. However, any kind

of resin may be used only if patterning and selective metal plating can be done on the resin.

Also, for ease of selective plating, the resins as described above with a plating catalyst contained therein may be used as in an embodiment.

However, the resin needs to be selected with sufficient consideration because of the difficulty in ensuring the adhesion between the ground resin film 2 and the plating material.

(Second Step)

Next, as shown in Fig. 1B, the ground resin film 2 obtained by the first step is subjected to exposure and development processes, thereby patterned into a wiring pattern. More specifically, as in the patterning of resist, after the ground resin film 2 is exposed to light (exposure level: 400 mJ/cm^2) by using a photomask with exposure equipment such as a stepper, a development process (for 50 seconds at room temperature) is performed with an alkali developer (PL-DEVELOPER-2N made by Hitachi Chemical - Du Pont), and then a baking process (for 60 min. at 300°C) is done. The film thickness of photosensitive polyimide at this time point is about 0.5 μm. This film thickness can be easily controlled by the rotation number of the spinner for the spin coating.

Photosensitive resins that can be patterned by exposure and development processes are optimal in terms of cost reduction and process simplification.

In addition, the ground resin referred to in this case may be made of novolak resin that is used as resist, polyimide-base or acrylic resin, epoxy resin that is used as printed wiring boards, and the like. However, any kind of photosensitive resin may be used only if selective wet film formation can be done on the resin.

However, the resin needs to be selected with sufficient consideration because of the difficulty in ensuring the adhesion between the ground resin and the plating material.

(Third Step)

Next, as shown in Fig. 1C, on the top surface of the ground resin film 2a patterned into a wiring pattern, a low-resistance metal film 3 is formed by electroless plating. In this case, Cu plating was used as the electroless plating, and Melplate Cu-390 made by Meltex Company was used as the plating solution. With this plating solution, a 10-min. plating process was performed at a solution temperature of 40°, by which a Cu thin film having a film thickness of 0.2 μm was obtained. The metal film to be formed by electroless plating may be made of copper, nickel, tin, gold, silver, chromium, palladium, or

the like. The thickness of this metal film may be set optionally by changing the immersion time into the plating solution.

For metal wirings in active matrix drive type LCDs, Cu is optimal in terms of material cost, resistance value, resistance to electromigration, and the like. Forming a film of Cu at a film thickness of 0.2 - 0.5 μm allows sufficiently low resistance for wirings, or interconnections, to be obtained.

Even in the case where there is no room for selection of the ground resin and where a low adhesion between the ground resin and the plated Cu is involved, low-resistance wirings having a good adhesion with the ground resin can be implemented by laying Ni, which allows the adhesion with the ground resin to be taken relatively easily, on the ground resin, and further thereon laying Cu/Au or the like.

Although electroless plating is used to form the low-resistance metal film in this embodiment, other wet film formation techniques such as electrolytic plating and electrodeposition may also be used. Using electrolytic plating allows a higher quality film of better adhesion with the ground film to be obtained, as compared with electroless plating.

As shown above, the metal wiring fabricating method of the first embodiment is capable of simplifying the manufacturing process to a large extent and fabricating the metal wirings with low cost as described below, as compared with the conventional method in which metal film of Ta or the like is used as the ground film and a low-resistance metal film is formed thereon.

Prior art manufacturing method: dry film formation process of ground metal film of Ta → photolithography process for patterning of ground metal film of Ta (resist coating, exposure, development) → etching (dry etching for Ta) → dry film formation process of low-resistance metal film of Cu → photolithography process for patterning of low-resistance metal film of Cu (resist coating, exposure, development) → etching (wet etching of Cu).

First embodiment manufacturing method: coating process of ground resin film → photolithography process for patterning of ground resin film (exposure, development) → electroless selective plating process of low-resistance metal film of Cu.

The plating process used in the first embodiment is electroless selective plating (in which no current is passed through the plating solution or the substrate, the metal film can be formed only by immersing the substrate

into the solution), thus making it easy to treat large-scale substrates.

Fig. 2 shows a cross-sectional structure of a thin film transistor (TFT) in which metal wirings manufactured by the fabrication process shown in Figs. 1A - 1C are applied to an active matrix substrate.

A gate line 11 is formed of a photosensitive polyimide film 13 as a ground resin film and a low-resistance metal film 14 made of Cu, on a glass substrate 12 which is an insulating substrate. Sheet resistance of this lamination film 11 is not more than 0.1 Ω/□. On the gate line 11, a gate insulator 15 made of SiNx is formed by CVD process (Chemical Vapor Deposition). Further on the gate insulator 15, are provided an a-Si film 16 as a channel portion, an n^+-type a-Si film 17 as a contact layer, a source electrode 18 and a drain electrode 19 made of Al, a pixel electrode 20 made of ITO, and an insulating overcoat 21 made of SiNx.

It was verified that the TFT device obtained in this way exhibit characteristics similar to those of conventional TFT devices using a gate line formed only by conventional dry film deposition. Thus, it was verified that the first embodiment is applicable to active matrix drive type LCDs.

(Second Embodiment)

In a second embodiment of the metal wiring fabricating method of the present invention, a plating technique and a film formation technique shown in Japanese Patent Laid-Open Publication HEI 10-245444 are used as wet film formation techniques.

At first and second steps, processes similar to those of the first embodiment are performed.

However, photosensitive polyimide is used as the resin for the first step. The surface of this polyimide is sulfonated by sulfuric acid in hydrogen peroxide solution or acetic anhydride, by which sulfo groups are introduced to the surface of the polyimide. Through neutralization of this, the sulfo groups are treated by a metal-ion containing solution so as to be transformed into metal salts of sulfo groups. The resulting metal ions are reduced so that a metal coating is formed on the surface of polyimide. By the method described above, a film of Cu is formed on the surface of the polyimide resin.

In this case, in order to make this film further lower in resistance, a film thickening process for the film of Cu was performed by using a plating technique, so that Cu/polyimide surface resistance was set to 0.1 Ω/□.

According to this method, a film which has no problems in terms of resistance for use as wiring lines for

large-scale, high-definition flat panel displays can be fabricated.

Also, by virtue of the use of polyimide, which is higher in heat resistance and chemical resistance as a resin film, such applications to TFTs as described in the first embodiment are allowed with ease also in the second embodiment.

(Third Embodiment)

This third embodiment includes, in addition to the steps of the metal wiring fabricating method of the first embodiment, a step for modifying the surface of the ground resin film.

Figs. 3A, 3B, 3C are process diagrams showing a method for fabricating metal wirings according to the third embodiment, where electroless plating is used as a wet film formation technique.

(First Step)

At a first step shown in Fig. 3A, after the surface of an insulating substrate 1 is cleaned and dried, photosensitive polyimide is applied to a thickness of 2.6 μm and then pre-baked (at 85°C for 120 seconds), by which a ground resin film 2 is formed.

(Second Step)

Next, at a second step shown in Fig. 3B, the ground resin film 2 is patterned. More specifically, the

ground resin film 2 made of photosensitive polyimide is exposed to light (exposure level: 400 mJ/cm^2) by using a photomask with exposure equipment such as a stepper. Thereafter, a development process (for 50 seconds at room temperature) is performed with an alkali developer (PL-DEVELOPER-2N made by Hitachi Chemical - Du Pont), and then a baking process (for 60 min. at 300°C) is done. The film thickness of a patterned ground resin film 2a at this time point is about 1 μm.

(Third Step)

Next, as shown in Fig. 3C, after the surface of the ground resin film 2a patterned into a wiring pattern is modified, a metal layer 4 is formed.

First, the ground resin film 2a made of photosensitive polyimide is immersed into a KOH solution (5 mol/L) (at 50°C and for 5 min.), thereby its surface being modified to have asperity. Through treatment with KOH, amide bonds and carboxyl groups, which are cation-exchange groups of photosensitive polyimide resin, are formed. It is noted that the film thickness of the ground resin film 2a at this time point is 0.3 μm.

Next, the insulating substrate 1 having the patterned ground resin film 2a is immersed into an $AgNO_3$ solution at room temperature and for 1 min. In this process, Ag ions are adsorbed to the modified surface 2b of

the ground resin film 2a by ion exchange reaction. Thereafter, the insulating substrate 1 having the ground resin film 2a is irradiated with ultraviolet rays (for two hours by a 140 W low-pressure mercury lamp), thereby making Ag ions reduced, by which a Ag layer 4 as the metal layer is formed on the ground resin film 2a.

Although the Ag layer 4 is formed as the metal layer in this embodiment, Cu, Pd or the like other than Ag may be used, and any metal layer will do only if the metal layer acts as a catalyst in electroless plating for forming a low-resistance metal film during the subsequent process. Also, when the low-resistance metal film is deposited by electroplating, a metal layer having such a low electric resistance that the surface resistance distribution becomes smaller is preferable.

Also in this embodiment, ultraviolet rays are irradiated to the entire surface of the insulating substrate 1, so that the Ag ions that have been adsorbed to the modified surface 2b of the ground resin film 2a are reduced. Alternatively, Ag ions may be selectively reduced by selectively irradiating ultraviolet rays, for example, with a mask or the like. In this case, the low-resistance metal film is not deposited at portions where Ag ions have not been reduced, low-resistance metal wirings with different constitutions can be formed on the patterned

ground resin film 2a. Further, Ag ions may be reduced by using a reducing agent without using ultraviolet rays.

(Fourth Step)

Next, as shown in Fig. 3D, a low-resistance metal film 3 is formed by electroless plating on the surface of the ground resin film 2a. In this case, Cu plating was used as the electroless plating, and Melplate Cu-390 made by Meltex Company was used as the plating solution. With this plating solution, a 10-min. plating process was performed at a solution temperature of 40°, by which a Cu thin film having a film thickness of 0.2 μm was obtained. The Ag layer 4 at the surface of the ground resin film 2a acts as a catalyst for Cu deposition. In this embodiment, because the Ag layer 4 was formed on the entire surface of the ground resin film 2a, Cu was deposited as the low-resistance metal film 3 on the entire surface of the ground resin film 2a.

In this embodiment, the film thickness of photosensitive polyimide, which is the ground resin film 2a, is about 0.3 μm and the film thickness of the Cu thin film, which is the low-resistance metal film 3, is about 0.2 μm. The sum of the thickness of the ground resin film 2a and the thickness of the low-resistance metal film 3, i.e., the total thickness of the metal wirings is about 0.5 μm. These metal wirings are preferable as metal wirings of

a thin film transistor (TFT) having the cross-sectional structure shown in Fig. 2. That is, since the thickness of the whole metal wirings is about 0.5 μm, which is an optimum thickness that makes it possible to avoid such problems as disconnections at wiring jumping portions or occurrence of cracks at edge portions, an active matrix drive type LCD superior in display grade can be realized.

Although the surface of the patterned ground resin film 2a is modified after the patterning of the ground resin film 2 in this embodiment, the surface of the ground resin film 2 prior to the patterning may be modified.

The present invention is suitable for flat panel displays such as liquid crystal displays (LCDs), plasma display panels (PDPs), electrochromic displays (ECDs) and electroluminescent displays (ELDs), and quite effective for cases where reduction in manufacturing cost by manufacturing process reduction or the use of Cu for lowering the wiring resistance is desired, and where wet film formation is desired in place of dry film deposition with a view to the saving of resources.

Further, the present invention is not limited to the method for fabricating metal wirings for flat panel displays, and may be widely used as a method for fabricating metal wirings in other fields.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A method for fabricating metal wirings, comprising the steps of:

forming a ground resin film by applying a resin onto an insulating substrate;

patterning the ground resin film; and

forming a low-resistance metal film selectively on the patterned ground resin film by a wet film formation technique.

2. A method according to Claim 1, wherein the ground resin film is made of a photosensitive resin that can be patterned by exposure and development.

3. A method according to Claim 1, wherein the low-resistance metal film is a single layer film containing any one of Cu, Ni and Au or a multilayer film containing at least one of these single layers.

4. A method according to Claim 1, wherein the ground resin film is made of polyimide.

5. A method according to Claim 1, wherein plating is used as the wet film formation technique, and the ground resin contains a plating catalyst.

6. A method according to Claim 1, further comprising:

a step for, before the step of forming the low-resistance metal film, modifying a surface of the ground resin film.

7. A method according to Claim 6, further comprising:

a step for, after the step of modifying the surface of the patterned ground resin film, forming on the surface-modified ground resin film a metal layer serving as a catalyst in the process of forming the low-resistance metal film by the wet film formation technique.

8. A method according to Claim 7, wherein the step of forming the metal layer acting as a catalyst in the process of forming the low-resistance metal film by the wet film formation technique comprises the steps of:

making metal ions adsorbed onto the surface-modified ground resin film; and

reducing the metal ions.

9. A method according to Claim 6, wherein the ground resin film is made of a photosensitive resin which can be patterned by exposure and development.

10. A method according to Claim 6, wherein the low-resistance metal film is a single layer film containing any one of Cu, Ni and Au or a multilayer film containing at least one of these single layers.

11. A method according to Claim 6, wherein the ground resin film is made of polyimide.

12. The metal wiring fabricating method according to Claim 11, wherein the step of modifying the surface of the patterned ground resin film is a process using KOH.

13. A method according to Claim 8, wherein

the metal ions to be adsorbed onto the surface-modified ground resin film are any one of Cu, Ag and Pd ions.

14. A method according to Claim 8, wherein

the step of reducing the metal ions is a process in which ultraviolet rays are irradiated to places where the low-resistance metal film is to be formed, by which the metal ions are selectively reduced.

ABSTRACT OF THE DISCLOSURE

There is provided a method for fabricating electrical wirings capable of being manufactured with low cost and easily applied to large-scale substrates. A photosensitive ground resin film is formed on an insulating substrate by coating process. The ground resin film is subjected to exposure and development processes, by which a ground resin film patterned into a wiring pattern is obtained. Then, on the patterned ground resin film, a low-resistance metal film made of Cu is formed by electroless plating.

Fig.1A

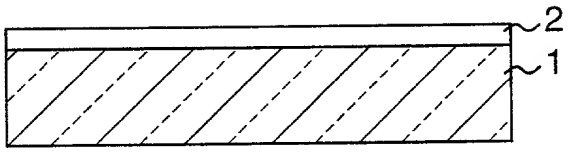


Fig.1B

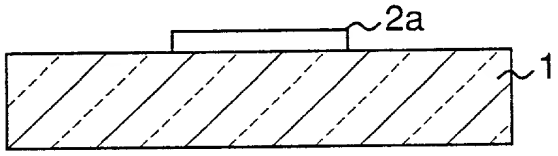


Fig.1C

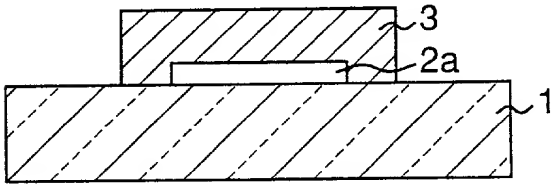


Fig.2

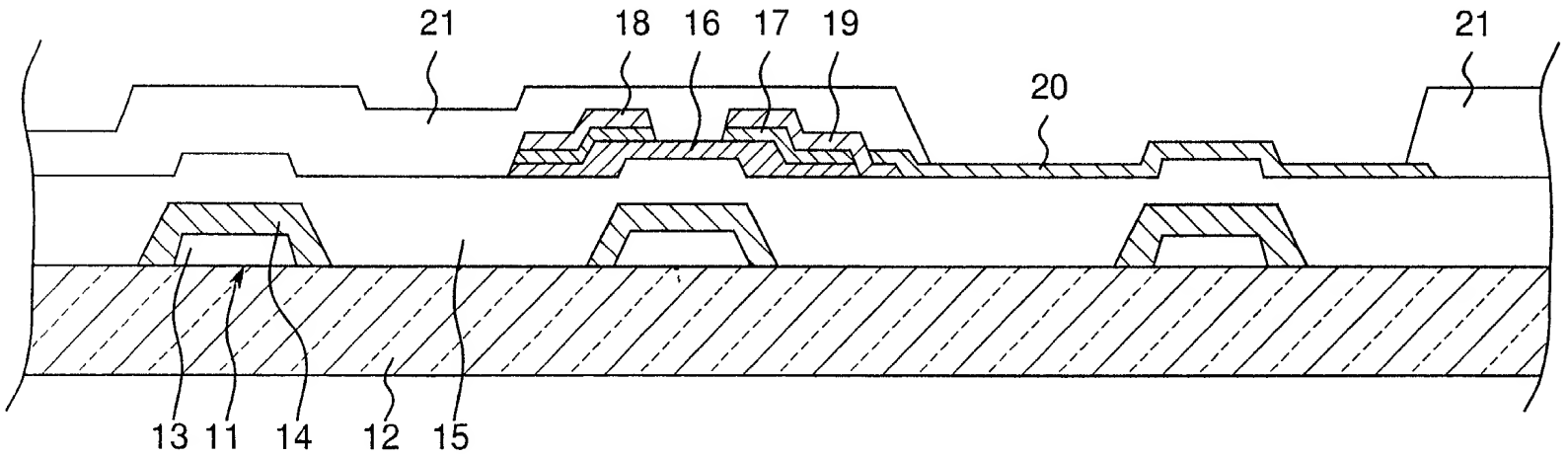


Fig.3A

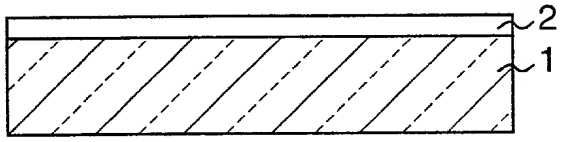


Fig.3B

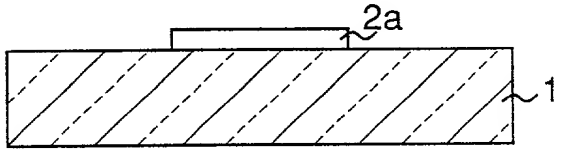


Fig.3C

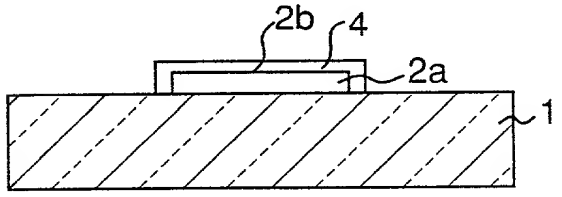
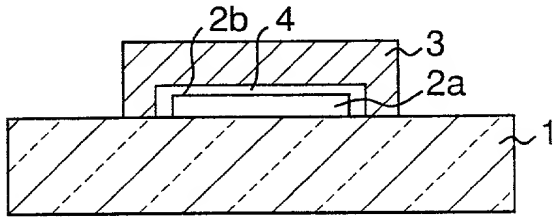


Fig.3D



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DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that: My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed at 201) below or an original, first and joint inventor (if plural names are listed at 201-208 below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR FABRICATING METAL WIRINGS

which is described and claimed in:

☒ the specification attached hereto.

☐ the specification in U.S. Application Serial Number _____, filed on _____.

☐ the specification in PCT international application Number _____, filed on _____; and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a). I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign/PCT Applications and Any Priority Claims Under 35 U.S.C. 119:			
Application No.	**Filing Date**	**Country**	**Priority Claimed Under 35 U.S.C. 119?**
11-239682	August 26, 1999	Japan	☒YES ☐NO
2000-205190	July 6, 2000	Japan	☒YES ☐NO
			☐YES ☐NO
			☐YES ☐NO
			☐YES ☐NO
			☐YES ☐NO
			☐YES ☐NO

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below, and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose material information as defined in 37 CFR §1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Prior U.S. Applications or PCT International Applications Designating the U.S-Benefit Under 35 U.S.C. §120				
U.S. Applications		Status (Check One)		
Application Serial No.	U.S. Filing Date	Patented	Pending	Abandoned
PCT Applications Designating the U.S.				
Application No.	Filing Date	U.S. Serial No. Assigned		

CLAIM FOR BENEFIT OF PRIOR U.S. PROVISIONAL APPLICATION(S)
(35 U.S.C. § 119(e))

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

Applicant	Provisional Application Number	Filing Date

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) with full powers of association, substitution and revocation to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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205	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
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	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY AND ZIP CODE

206	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
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207	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
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	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY AND ZIP CODE

208	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
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	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY AND ZIP CODE

I hereby further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signature of Inventor 201 Yoshimasa Chikama	Signature of Inventor 202 Yoshihiro Izumi
Date: August 7, 2000	Date: August 7, 2000